WHAT IS CLAIMED IS:

1. A bidirectional shift register comprising:

an output circuit that includes a first transistor having a conductive path between a first clock terminal and an output terminal and a second transistor having a conductive path between a power supply electrode and the output terminal;

an input circuit that includes a third transistor having a conductive path between a forward direction pulse input terminal and a control electrode of the first transistor, a fourth transistor having a conductive path between a backward direction pulse input terminal and the control electrode of the first transistor and a fifth transistor having a conductive path between the power supply electrode and a control electrode of the second transistor;

a reset circuit that includes a sixth transistor having a conductive path between a second clock terminal and the control electrode of the second transistor, a seventh transistor having a conductive path between a third clock terminal and the control electrode of the second transistor and an eighth transistor having a conductive path between the power supply electrode and the control electrode of the first transistor, which makes the path between the sixth transistor, the control electrode of the second transistor and a control electrode of the eighth transistor conductive as well as making the path between the fifth transistor and the seventh transistor non-conductive in forward direction pulse shift and which makes the path between seventh transistor, the control electrode of the second transistor and the control electrode of the eighth transistor conductive as well as making the path between the fifth transistor and the sixth transistor non-conductive in backward direction pulse shift; and

an inversion preventing circuit that prevents inversion of a voltage level in the control electrode of the second transistor when a voltage level of a clock signal inputted to the first clock terminal is inverted in a state where the first transistor is on and the second transistor is off.

2. The bidirectional shift register of Claim 1, wherein the input circuit includes an eleventh transistor having a conductive path between the third transistor and the control electrode of the first transistor, a twelfth transistor having a conductive path between the fourth transistor and the first transistor, a thirteenth transistor having a conductive path between the forward direction pulse input terminal and the fifth transistor and a fourteenth transistor having a conductive path between the backward direction pulse input terminal and the fifth transistor, turns on the eleventh transistor and the thirteenth transistor as well as turning off the twelfth transistor and the fourteenth transistor in the forward direction pulse shift and turns off the eleventh transistor and the thirteenth transistor as well as turning on the twelfth transistor and the fourteenth transistor in the backward direction pulse shift.

3. The bidirectional shift register of Claim 1, wherein the reset circuit includes a fifteenth transistor having a conductive path between the sixth transistor, the second transistor and the eighth transistor and a sixteenth transistor having a conductive path between the seventh transistor, the second transistor and the eighth transistor, turns on the fifteenth transistor as well as turning off the sixteenth transistor in the forward direction pulse shift and turns off the fifteenth transistor as well as turning on the sixteenth transistor in the backward direction pulse shift.

4. The bidirectional shift register of Claim 1, wherein the inversion

prevention circuit includes a ninth transistor having a conductive path between the power supply electrode and the control electrode of the second transistor and a conductive path to the control electrode of the first transistor and a tenth transistor having a conductive path between the ninth transistor and the second transistor and a conductive path to the first clock terminal, supplies a power supply voltage to the control electrode of the second transistor by turning on both of the ninth and tenth transistors when a voltage level of a clock signal inputted to the first clock terminal is inverted in a state where the first transistor is on and the second transistor is off.

5. A drive circuit comprising:

a plurality of bidirectional shift registers which are connected to each other in such a manner that an output signal from an output terminal of each of the bidirectional shift registers is inputted to a backward direction pulse input terminal of the bidirectional shift register in a preceding stage as well as to a forward direction pulse input terminal of the bidirectional shift register in a subsequent stage, each bidirectional shift register including

an output circuit that includes a first transistor having a conductive path between a first clock terminal and an output terminal and a second transistor having a conductive path between a power supply electrode and the output terminal,

an input circuit that includes a third transistor having a conductive path between a forward direction pulse input terminal and a control electrode of the first transistor, a fourth transistor having a conductive path between a backward direction pulse input terminal and the control electrode of the first transistor and a fifth transistor having a conductive path between the power supply electrode and a control electrode of the second transistor,

a reset circuit that includes a sixth transistor having a conductive path between a second clock terminal and the control electrode of the second transistor, a seventh transistor having a conductive path between a third clock terminal and the control electrode of the second transistor and an eighth transistor having a conductive path between the power supply electrode and the control electrode of the first transistor, which makes the path between the sixth transistor, the control electrode of the second transistor and a control electrode of the eighth transistor conductive as well as making the path between the fifth transistor and the seventh transistor non-conductive in forward direction pulse shift and which makes the path between the seventh transistor, the control electrode of the second transistor and the control electrode of the eighth transistor conductive as well as making the path between the fifth transistor and the sixth transistor non-conductive in backward direction pulse shift and

an inversion prevention circuit that prevents inversion of a voltage level in the control electrode of the second transistor when a voltage level of a clock signal inputted to the first clock terminal is inverted in a state where the first transistor is on and the second transistor is off.

6. The drive circuit of Claim 5, wherein the input circuit includes an eleventh transistor having a conductive path between the third transistor and the control electrode of the first transistor, a twelfth transistor having a conductive path between the fourth transistor and the first transistor, a thirteenth transistor having a conductive path between the forward direction pulse input terminal and the fifth transistor and a fourteenth transistor having a conductive path between the backward direction pulse input terminal and the fifth transistor, turns on the eleventh transistor and the

thirteenth transistor as well as turning off the twelfth transistor and the fourteenth transistor in the forward direction pulse shift and turns off the eleventh transistor and the thirteenth transistor as well as turning on the twelfth transistor and the fourteenth transistor in the backward direction pulse shift.

7. The drive circuit of Claim 5, wherein the reset circuit includes a fifteenth transistor having a conductive path between the sixth transistor, the second transistor and the eighth transistor and a sixteenth transistor having a conductive path between the seventh transistor, the second transistor and the eighth transistor, turns on the fifteenth transistor as well as turning off the sixteenth transistor in the forward direction pulse shift and turns off the fifteenth transistor as well as turning on the sixteenth transistor in the backward direction pulse shift.

8. The drive circuit of Claim 5, wherein the inversion prevention circuit includes a ninth transistor having a conductive path between the power supply electrode and the control electrode of the second transistor and a conductive path to the control electrode of the first transistor and a tenth transistor having a conductive path between the ninth transistor and the second transistor and a conductive path to the first clock terminal, supplies a power supply voltage to the control electrode of the second transistor by turning on both of the ninth and tenth transistors when a voltage level of a clock signal inputted to the first clock terminal is inverted in a state where the first transistor is on and the second transistor is off.

9. A flat display device comprising:

a plurality of bidirectional shift registers in at least one of a scan line drive circuit and a signal line drive circuit, the bidirectional shift registers

being connected to each other in such a manner that an output signal from an output terminal of each of the bidirectional shift registers is inputted to a backward direction pulse input terminal of the bidirectional shift register in a preceding stage as well as to a forward direction pulse input terminal of the bidirectional shift register in a subsequent stage and each bidirectional shift register including

an output circuit that includes a first transistor having a conductive path between a first clock terminal and an output terminal and a second transistor having a conductive path between a power supply electrode and the output terminal,

an input circuit that includes a third transistor having a conductive path between a forward direction pulse input terminal and a control electrode of the first transistor, a fourth transistor having a conductive path between a backward direction pulse input terminal and the control electrode of the first transistor and a fifth transistor having a conductive path between the power supply electrode and a control electrode of the second transistor,

a reset circuit that includes a sixth transistor having a conductive path between a second clock terminal and the control electrode of the second transistor, a seventh transistor having a conductive path between a third clock terminal and the control electrode of the second transistor and an eighth transistor having a conductive path between the power supply electrode and the control electrode of the first transistor, which makes the path between the sixth transistor, the control electrode of the second transistor and a control electrode of the eighth transistor conductive as well as making the path between the fifth transistor and the seventh transistor non-conductive in forward direction pulse shift and which makes the path

between the seventh transistor, the control electrode of the second transistor and the control electrode of the eighth transistor conductive as well as making the path between the fifth transistor and the sixth transistor non-conductive in backward direction pulse shift and

an inversion prevention circuit that prevents inversion of a voltage level in the control electrode of the second transistor when a voltage level of a clock signal inputted to the first clock terminal is inverted in a state where the first transistor is on and the second transistor is off;

an array substrate including the scan line drive circuit, the signal line drive circuit, switching elements and pixel electrodes provided in the respective switching elements, the switching elements being provided at respective intersections of a plurality of scan lines from the scan line drive circuit and a plurality of signal lines from the signal line drive circuit;

a counter substrate which is disposed opposite to the array substrate and has counter electrodes provided thereon, the counter electrodes electrically corresponding to the respective pixel electrodes; and

a display layer held between the array substrate and the counter substrate.

10. The flat display device of Claim 9, wherein the input circuit includes an eleventh transistor having a conductive path between the third transistor and the control electrode of the first transistor, a twelfth transistor having a conductive path between the fourth transistor and the first transistor, a thirteenth transistor having a conductive path between the forward direction pulse input terminal and the fifth transistor and a fourteenth transistor having a conductive path between the backward direction pulse input terminal and the fifth transistor, turns on the eleventh transistor and the

thirteenth transistor as well as turning off the twelfth transistor and the fourteenth transistor in the forward direction pulse shift and turns off the eleventh transistor and the thirteenth transistor as well as turning on the twelfth transistor and the fourteenth transistor in the backward direction pulse shift.

11. The flat display device of Claim 9, wherein the reset circuit includes a fifteenth transistor having a conductive path between the sixth transistor, the second transistor and the eighth transistor and a sixteenth transistor having a conductive path between the seventh transistor, the second transistor and the eighth transistor, turns on the fifteenth transistor as well as turning off the sixteenth transistor in the forward direction pulse shift and turns off the fifteenth transistor as well as turning on the sixteenth transistor in the backward direction pulse shift.

12. The flat display device of Claim 9, wherein the inversion prevention circuit includes a ninth transistor having a conductive path between the power supply electrode and the control electrode of the second transistor and a conductive path to the control electrode of the first transistor and a tenth transistor having a conductive path between the ninth transistor and the second transistor and a conductive path to the first clock terminal, supplies a power supply voltage to the control electrode of the second transistor by turning on both of the ninth and tenth transistors when a voltage level of a clock signal inputted to the first clock terminal is inverted in a state where the first transistor is on and the second transistor is off.

13. A bidirectional shift register comprising:

an input circuit in which a pulse is inputted to a fifth transistor

having a conductive path between a power supply electrode and a second transistor;

an output circuit configured to output the clock signal inputted to the first clock terminal by a first transistor, and output a power supply voltage by the second transistor;

a reset circuit configured to make the path between a second clock terminal and the fifth transistor conductive as well as making the path between a third clock terminal and the fifth transistor non-conductive in forward direction pulse shift, to make the path between the second clock terminal and the fifth transistor non-conductive as well as making the path between the third clock terminal and the fifth transistor conductive in backward direction pulse shift; and

an inversion prevention circuit that prevents inversion of a voltage level in the control electrode of the second transistor when a voltage level of a clock signal inputted to the first clock terminal is inverted in a state where the first transistor is on and the second transistor is off.